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Dated 9 December 2003

Patents Form 1/77

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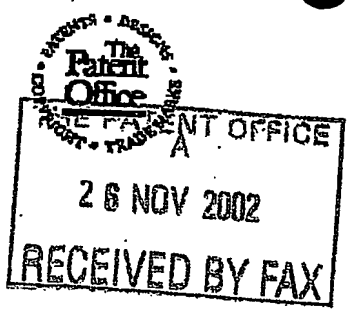

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Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

The Patent Office
Cardiff Road
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26 NOV 2002

1. Your reference — RH/SEB/P/75829.GB/S

27NOV02 E766360-1 D02802
P01/7700 0.00-0227526.1

2. Patent application number *(The Patent Office will fill in this part)* — 0227526.1

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

MELEXIS NV
Microelectronic Integrated Systems
Rozendaalstraat 12
B-8900 Ieper
Belgium

Patents ADP number *(if you know it)*

If the applicant is a corporate body, give the country/state of its incorporation — Belgium Corporation

8351702001

4. Title of the invention — AUTO-CONFIGURED LIN BUS NODES

5. Name of your agent *(if you have one)*

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

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148/9 GREAT CHARLES STREET
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UNITED KINGDOM

Patents ADP number *(if you know it)* — 7710734001

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day / month / year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

a)

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9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	
Description	10 (p.s.m)
Claim(s)	
Abstract	
Drawing(s)	3 only

10. If you are also filing any of the following, state how many against each item.

Priority documents	
Translations of priority documents	
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	
Request for preliminary examination and search *(Patents Form 9/77)*	
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application.

Signature [signature] Date 26 November 2002

12. Name and daytime telephone number of person to contact in the United Kingdom

Mr R Hill
0121 236 1038

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b) *Write your answers in capital letters using black ink or you may type them.*

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AUTO-CONFIGURED LIN BUS NODES

The invention relates to electronic devices and more specifically to electronic devices used within systems conforming to the LIN Bus standard.

Lin Bus is a name given to an open protocol defined for use in communicating between a number of distributed modules. Many applications of the Lin Bus are targeted specifically at the automotive industry.

In Lin Bus applications each module contains an interface circuit, usually implemented as a single integrated circuit, which interfaces to the common signal conductor or BUS and handles the protocols associated with the messages and the required responses.

Each modules in a system has a unique identity,ID, within the system, which enables a bus master to communicate with a selected module or a group of modules within the system.

As originally defined, all the modules within a LIN Bus system are connected in parallel. That is they share a BUS across which all messages and communications are sent and received. Each module has a pull up resistor and an active pull down transistor. Message initiation is asynchronous and message collisions are resolved by arbitration means. Since a pull down or active state, will take precedance over a pull up, or recessive state, any transmitting module seeing an active state when transmitting a recessive state knows that another module is transmitting. Under such circumstances the module transmitting the active state takes precedence and any other modules must cede the bus and try again later.

Each module is assumed to be preconfigured before installation each with its own unique ID.

Such an assumption places demands on the manufacturers, installers and more especially on a system repairers to correctly configure every module before installing it into the system. An extension to the system protocol providing thereby a method of configuring a module with an ID after installation was proposed and implemented by Bosch and Philips amongst others and has been favorably received.

Such an extended system permits modification of the electronic interface. The single connection from each module to the BUS is replaced by two connections. The BUS is made discontinuous at each extended capability module and one connection is made to each side of the discontinuity. Extended capability modules are thus connected in a daisy chain configuration whilst normal modules are connected to the BUS as before. Each extended capability module maintains signal continuity along the BUS but introduces a nominal (approximately one ohm) series resistance per extended capability module. Extended capability modules are manufactured in a non configured state but can be configured after installation. In a non configured state a module has no ID and therefore cannot be selectively communicated with and thus given an ID. To overcome this limitation, all un-configured extended capability modules respond to a configuration request message transmitted onto the BUS by a bus master, by turning off their pull down transistors and forcing a current thorough their pull up resistor onto the common signal conductor. These forced currents will flow along the common signal conductor to the bus master which has its pull down transistor turned on. By this means every un-configured extended capability module except one will see a voltage across the nominal one ohm series resistance introduced at each extended capability module. The exception is the module furthest from the master as defined by the daisy chaining connections. This un-configured extended capability module is thus uniquely identified and enables itself for programming of an ID within the system. The procedure can be repeated until all un-configured extended capability modules are configured with an ID.

Such a scheme has a number of limitations. The normal performance of the bus is degraded by the introduction of the series resistances. The series resistance within an extended capability module is normally implemented within an integrated circuit and the tolerance of such

resistors is wide. The forced currents are all sunk via the bus master, which has maximum current capabilities and a current limiting capability defined within the specification. The value of the forced current used to identify and enable one module for configuration must be small and carefully selected and controlled. The voltages developed across the series resistor within a module are also small and must be measured with high accuracy.

A better solution is needed that can deliver the benefits of simple selection of one of a number of an un-configured extended capability module for configuration whilst imposing the fewest restraints on the tolerances of the individual elements of the implementation of the system and maintaining compatibility with the LIN bus specification.

According to a first aspect of the present invention there is provided a reconfigurable module having means for being configured with an ID and also having embedded within it at the manufacturing stage a fixed unique Chip Identification Code, CIN, for use during a configuring operation.

According to a second aspect of the present invention there is provided a LIN bus system comprising a plurality of modules linked to a LIN bus along which electronic data or instructions can be sent to and from each said module, at least one of said modules being non configured and having no unique identification address associated therewith, said at least one module having a unique code associated therewith, said system further including configuration means which interrogates said modules and detects the unique code of said at east one non configured module and transmits a configuration signal to the module to configure the module, each said non configured module including counter means which is incremented each time a non configured module is configured, said counter of each non configured module, once configured, providing a unique code which is indicative of the position of the module in the system.

During a configuration sequence the bus master transmits a configuration request and all un-configured reconfigurable modules respond by transmitting a reply consisting of their CIN. The usual arbitration scheme will apply, with active states winning over recessive states. One un-

configured reconfigurable module will thus win the arbitration and become the 'selected device'. The selected device only then forces a current through the pull up resistor. Non selected un-configured reconfigurable modules will monitor the current through their series resistors to determine that a selected device is responding. Each un-configured reconfigurable module maintains a position counter. The position counter is incremented each time a selected device responds with a forced current. The position counter within any un-configured reconfigurable module will not be incremented when that un-configured extended capability module is itself the selected device. Once an un-configured reconfigurable module has been selected it is no longer considered un-configured and remains unresponsive to further configuration requests and with its position counter fixed showing its position in the daisy chain. Once all un-configured extended capability modules have been selected each will have a position counter showing a unique position for that module within the daisy chain. This unique position counter value can be used to select a module and configure it for use in the system.

The benefits of such an improved system are that only one module is forcing current at a time thus simplifying the task of determining that a current is flowing by reducing the accuracy required for the measurement. The tolerances of the components are also less onerous.

Fig 1 shows a block diagram of a module interface with the series resistance.

Fig 2 shows a plurality of modules connected to a common signal line.

Fig 3 illustrates the sequence of determining the positions within a daisy chain

The MLX90402 is an embodiment of the invention and can be described with reference to the figures.

Fig 1 shows a block diagram of a module interface with the series resistance. The normal LIN bus interface pin is split into a LIN_H pin, 101, and a LIN_L pin, 102, connected with a resistor Rac, 104, of typically 1 ohm This genables modules to be connected as a daisy chain of slave nodes on the LIN bus.

During the auto-configuration procedure the voltage across the resistor Rac is monitored. This is done by amplifier means, 107.

On the chip is also a pull up current source Iac, 105, which can be activated during auto-configuration. During normal communication this current source is always off and has therefore no influence. This current source has a typical value of 8 mA.

The LIN pull up resistor, 104, can also be switched off during the auto-configuration process.

Figure 2 shows an example of a daisy-chained LIN bus for auto-configuration.

The master module, 201, is located at one end of the bus. The modules 1 to n, 211..21n, are slave nodes with auto-configuration capability. The devices are daisy-chained by connecting the LIN_H pin.,101, to the device to the left and connecting the LIN_L pin, 102, to the device to the right. The device n+1, ... are standard slave modules. They can be connected anywhere on the LIN bus.

On the bus there can be any combination of slaves featuring the auto-configuration system with standard slave nodes. These standard slaves can be put anywhere on the bus. The bus can be a tree structure as far as the slaves with auto-configuration remain connected in a daisy-chain way.

The MLX90402 can have following auto-configuration states:

- *Unaddressed:* the node is not identified (i.e. the node has not assigned an ID and can thus not be accessed for normal messages requiring the ID of a node).
- *Selected:* the node has been selected during the on-going auto-configuration interrogation message. It will switch to the addressed state at the end of the message.
- *Addressed:* the node has been addressed during the auto-configuration procedure. It is waiting the end of the auto-configuration procedure to get assigned his node ID.

- *Identified:* the node has received his proper ID (which is written in eeprom) and can be accessed for all application messages.

A chip that has never been identified has ID=0 written in Non Volatile memory NVM. Such a chip will enter the unaddressed state after power on reset.

A chip that is not in the identified state will enter the unaddressed state after power on reset.

Every MLX90402 chip has a unique CIN (chip identification number) code built in at manufacture. This code can be any code, except a code consisting of all zeros. In practice this code consist of data defining batch No, wafer No and die position on the wafer.

The CIN has a total of 48 bits or 6 bytes of unique code.

No special hardware is required for the master. Any micro-processor equipped with a regular full duplex Uart, associated with a standard Lin physical interface circuit (such as the TH8082 from Melexis) can be used. The software running on the master must be able to send the frame items (Uart bytes) in a different way than for the regular frames.

The auto-configuration system makes use of the user defined extended frame message (Id 0x3E). The advantages of the usage of the extended frame are the following:

It leaves the regular Lin identifiers untouched and available.

The number of bytes is free; it can be optimized for each message.

The byte containing the error flag can be located at the end of the frame, after the checksum (to allow for signalling of checksum errors, by the master as well as the slaves).

The first byte of the extended frame is sent by the master and identifies one of the configuration frames (the following bytes depend on the function):

Id	First byte	Function	Following bytes	Last bytes
0x3E	1111 1111	UAD	2 data bytes	checksum
0x3E	1111 1110	INT	CIN:	Checksum & Flags
0x3E	1111 1101	IDS	ECU address byte,	Checksum & Flags
0x3E	1111 1100	FRQ	See Error! Reference source not found..	checksum
0x3E	1111 0 ---	Reserved for future use		

UAD: un-address all auto-configuration slaves

The UAD message is a regular message with data sent by the master When the master initiates the UAD command all auto-configuration slaves reset their node identifier ID to 0 and set their internal counter PosCnt to 1.

The result is that all slaves are now in the unaddressed state.

The bus is now ready to start the auto-configuration process.

INT: interrogate all auto-configuration slaves

The INT message is an extended message containing 8 bytes of data. When the master initiates this command, it is processed by all auto-configuration slaves who are in the unaddressed or addressed state.

During the first 6 bytes (Data 0 – 5), all unaddressed slaves send their CIN code in an arbitration fashion: if a slave detects a dominant level while trying to transmit a recessive level, it looses the arbitration and switches to a recessive level for the remaining of the CIN code transmission. During these bytes the master must send a data byte 0xFF (all recessive) to initiate the arbitration.

At the end of the CIN code transmission one and only one slave will have succeeded in transmitting his full CIN code and therefore recognises itself as selected. This slave will transmit the checksum to result in a correct message for all standard slaves. This selected slave will switch to the addressed state at the end of the message (if the checksum transmission and the error flag are correct).

During the next byte (Data 6), the master sends 8 dominant bits, while all auto-configuration slaves switch off their LIN pull up resistor.
- During the first 4 bits all auto-configuration slaves in the unaddressed state will calibrate on the bus. This means that the voltage across the resistor Rac is amplified and measure by the ADC. This will be used as a reference voltage during the next 4 bits.
- During the second 4 bits the selected slave will enable its current source Iac and all addressed and unaddressed slaves will monitor the voltage drop across their resistor Rac. If the voltage threshold is exceeded (i.e. the chip detects a current Iac), the slave will increment his internal counter PosCnt.

During the last Byte (Data 7) all unaddressed slaves send a dominant bit followed by a recessive bit (the addressed slaves and the selected slave do nothing). The master also sends a 0xFF byte to initiate the response from the slaves. This is the 'More' flag. It indicates that at least 1 slave is still in the unaddressed state.

The remaining 6 bits can be used to signal an error flag (a slave disagreeing with the configuration sequence sends 1 dominant bit followed by 5 recessive bits).

The message is completed by the selected slave sending the checksum. In case no slave responds (CIN is fully recessive), the master must send the corresponding checksum to still have a correct message.

At the end the selected slave switches to the addressed state if there was no error flag. If an error has been indicated the slave switches back to the unaddressed state.

The master will repeat this interrogation message until no configurable slaves are in the unaddressed state, i.e. until the 'More' flag is not returned.

The configuration is completed correctly if:

All checksums were correct.

No 'all recessive CIN code' was received.

No error flag was received.

The 'More' flag was transmitted correctly (for all messages but the last one).

Figure 3 shows an example of the sequence of this bus configuration. The bus consists of a master node, 5 slave nodes with auto-configuration feature, and 3 standard slave nodes.

The sequence of selection of the slave nodes depend on their CIN code; as an example a select sequence is chosen in the figure. Based on this sequence the value of the position counter (PosCnt) is shown after each auto-configuration cycle.

Slaves numbered 4, 5 and 8 are standard Lin nodes.

When the configuration process is completed, the internal counter PosCnt of each slave contains its position in the daisy chain. This value, the ECU address, is be used to configure the modules to suit the application.

It is of course to be understood that the invention is not intended to be restricted to the details of the above embodiment which is described by way of example only.

The CIN code (which is in eeprom) can also be replaced by a random generated code of x bits. The random generator is on chip. The right value for x is calculated to minimize the risk of having identical codes.

In case of identical codes, this does not need to be a problem for example if 2 slaves have identical codes, both are selected and they will both activate their current course. In this situation there are 2 possibilities:

- The selected slave closest to the master will also detect a current flowing through its resistor and therefore this slave will recognise that it is not the only slave and will react as if not selected.

- An error flag can be generated by the master or the selected slave closest to the master and restart the procedure.

The advantage of this alternative is that there is no need for non volatile memory on the chip since the configuration system can be run on power every time.

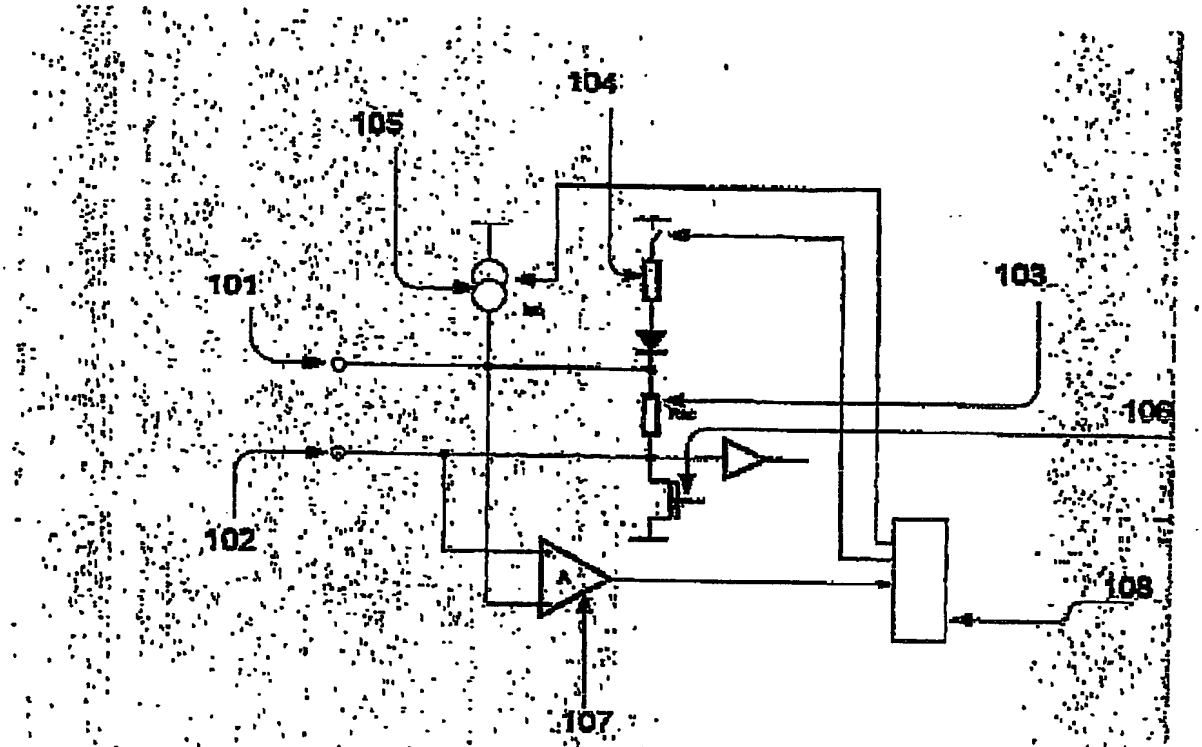

Figure 1

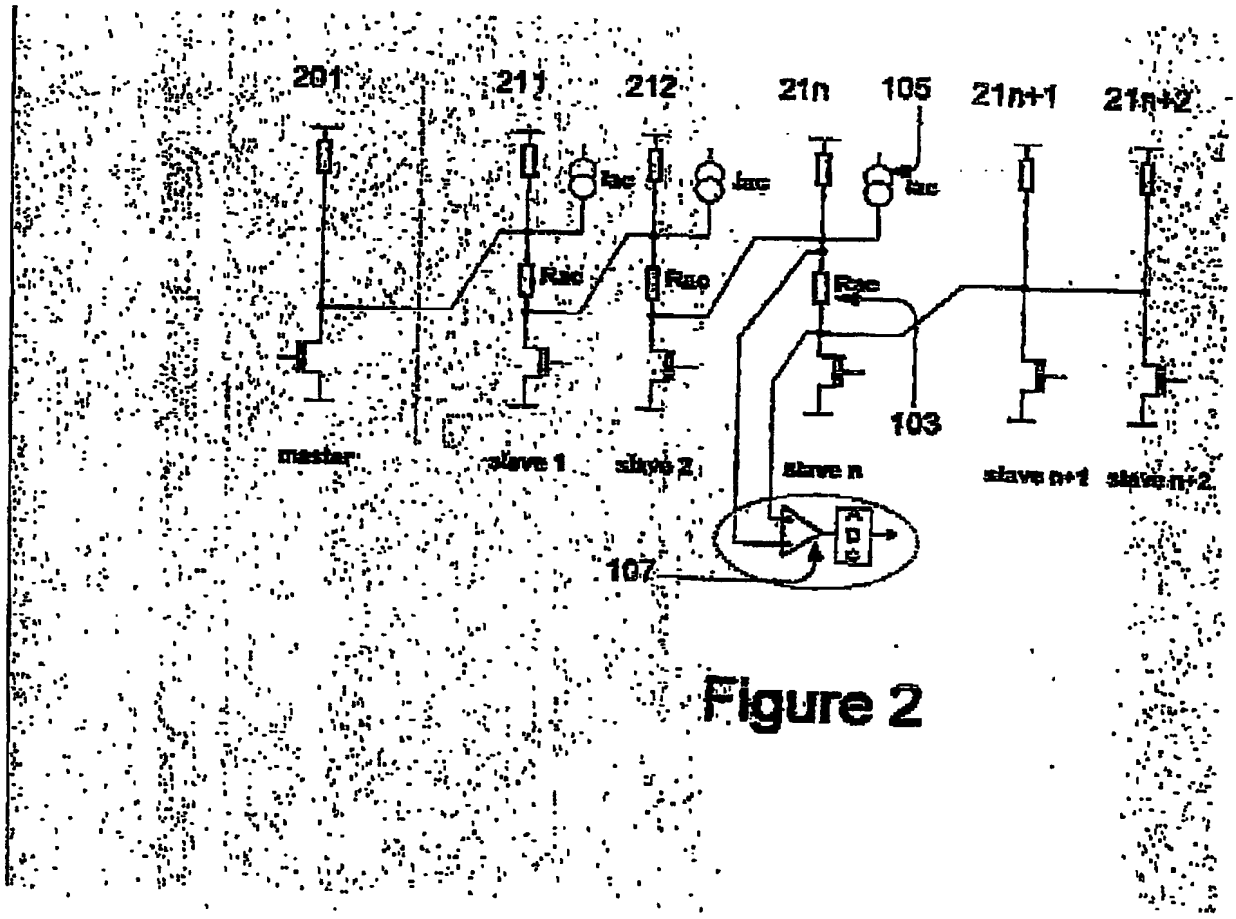
201
211
212
21n
105
21n+1
21n+2
Iac
Iac
Iac
Rac
Rac
Rac
103
master
slave 1
slave 2
slave n
slave n+1
slave n+2
107

Figure 2

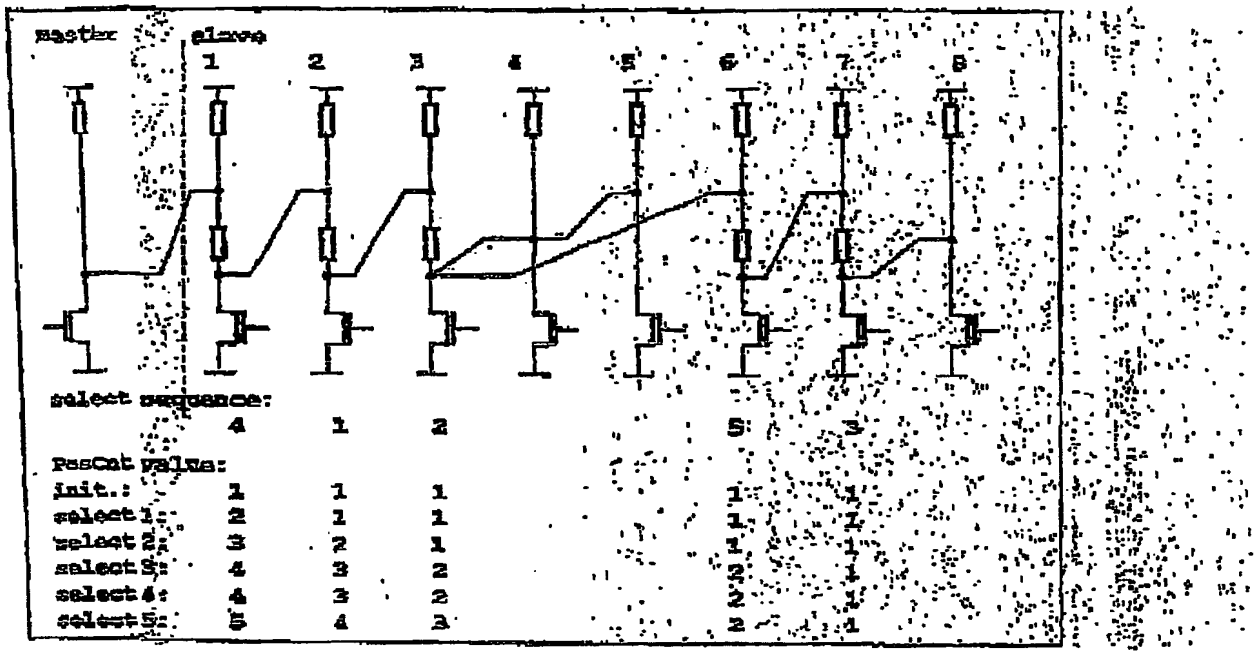
master
slaves
1 2 3 4 5 6 7 8
select sequence:
4 1 2 5 3
ResCat value:
init.: 1 1 1 1 1
select 1: 2 1 1 1 1
select 2: 3 2 1 1 1
select 3: 4 3 2 2 1
select 4: 4 3 2 2 1
select 5: 5 4 3 2 1

Figure 4